CLAIM AMENDMENTS

Please amend the claims by amending claims 28-29, without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment:

1.-23. (cancelled)

24. (previously presented) A method of operating an integrated circuit with nonvolatile memory cells comprising:

generating from a power source an operating voltage for a memory operation;

connecting said power source to nonvolatile memory cells selected for said memory operation via a node of nonvolatile memory cells;

floating said node after it has been charged substantially to said operating voltage; and

allowing said node to hold said operating voltage dynamically while performing said memory operation dynamically on the selected nonvolatile memory cells.

25. (previously presented) The method of claim 24, further comprising: periodically reconnecting said power source to said node to refresh the voltage on said node until the memory operation is completed.

26. (previously presented) The method of claim 25, wherein

said nonvolatile memory cells are organized in an array accessible by word lines and bit lines; and

said node is connected to a word line.

27. (previously presented) The method of claim 24, further comprising:

permitting another memory operation on nonvolatile memory cells, other than the nonvolatile memory cells selected for dynamic operation.

28. (amended) The method of claim 27 [~~26~~], wherein said another memory operation includes:

programming of nonvolatile memory cells, other than the nonvolatile memory cells selected for dynamic operation.

29. (amended) The method of claim 27 [~~26~~], wherein said another memory operation includes:

reading of nonvolatile memory cells, other than the nonvolatile memory cells selected for dynamic operation.

30. (previously presented) The method of claim 24, wherein each nonvolatile memory cell comprises one charge storage element.

31. (previously presented) The method of claim 24, wherein each nonvolatile memory cell comprises more than one charge storage element.

32. (previously presented) The method of claim 24 further comprising:

permitting other operations within the integrated circuit, other than operations on the nonvolatile memory cells selected for dynamic operation.

33. (previously presented) The method of claim 24, further comprising:

checking at predetermined times whether the selected nonvolatile memory cells have completed said dynamic memory operation; and

if the selected nonvolatile memory cells have not completed said dynamic memory operation, reconnecting said power source to refresh the voltage on said node.

34. (previously presented) The method of claim 33, further comprising:

after the selected nonvolatile memory cells have completed the dynamic memory operation, discharging said node to a predetermined voltage level.

35. (previously presented) A method of operating an integrated circuit comprising:

connecting an operating voltage to a first portion of nonvolatile memory cells;

charging a node of the first portion of nonvolatile memory cells to the operating voltage;

floating the node of the first portion of the memory cells to hold the operating voltage dynamically; and

operating on the first portion of nonvolatile memory cells dynamically.

36. (previously presented) The method of claim 35 further comprising:

while the first portion of nonvolatile memory cells is dynamically being operated on, permitting operation on a second portion of nonvolatile memory cells.

37. (previously presented) The method of any one of claims 24-36, wherein each nonvolatile memory cell stores one bit of data.

38. (previously presented) The method of any one of claims 24-36, wherein each nonvolatile memory cell stores more than one bit of data.

39. (previously presented) The method of any one of claims 24-36, wherein each nonvolatile memory cell includes a floating gate.

40. (previously presented) An nonvolatile memory comprising:

an array of memory cells arranged in rows and columns accessible by word lines and bit lines;

a transfer transistor coupled to individual word line; and

a power source coupled to a selected word line via an respective transfer transistor; and wherein said respective transfer transistor is enabled to charge interconnected gates along a row of memory cells to an operating voltage and said respective transfer transistor is disabled to hold the operating voltage dynamically at the word line.

41. (previously presented) The nonvolatile memory of claim 40, further comprising:

a control signal to enable or disable said transfer transistor, and said control signal further enabling said transfer transistor at predetermined times to allow coupling of said power source to refresh the voltage on the selected word line.

42. (previously presented) An integrated circuit with nonvolatile memory cells comprising:

means for generating from a power source an operating voltage for a memory operation;

means for connecting said power source to nonvolatile memory cells selected for said memory operation via a node of nonvolatile memory cells;

means for floating said node after it has been charged substantially to said operating voltage; and

means for allowing said node to hold said operating voltage dynamically while performing said memory operation dynamically on the selected nonvolatile memory cells.

43. (previously presented) The integrated circuit of claim 42, further comprising:

checking at predetermined times whether the selected nonvolatile memory cells have completed said dynamic memory operation; and

if the selected nonvolatile memory cells have not completed said dynamic memory operation, reconnecting said power source to refresh the voltage on said node.

44. (previously presented) An integrated circuit comprising:

means for connecting an operating voltage to a first portion of nonvolatile memory cells;

means for charging a node of the first portion of nonvolatile memory cells to the operating voltage;

means for floating the node of the first portion of the memory cells to hold the operating voltage dynamically; and

means for operating on the first portion of nonvolatile memory cells dynamically.

45. (previously presented) The integrated circuit of claim 44, further comprising:

while the first portion of nonvolatile memory cells is dynamically being operated on, permitting operation on a second portion of nonvolatile memory cells.

46. (previously presented) The integrated circuit of any one of claims 42-45, wherein each nonvolatile memory cell stores one bit of data.

47. (previously presented) The integrated circuit of any one of claims 42-45, wherein each nonvolatile memory cell stores more than one bit of data.

48. (previously presented) The integrated circuit of any one of claims 42-45, wherein each nonvolatile memory cell includes a floating gate.